

Genie Ethernet Verification IP

The **Perfectus Ethernet VIP** provides a quick and efficient way to verify System on chip (SOC), ASIC designs for ethernet interface. The VIP is compliant with IEEE 802.3 standard. The VIP for Ethernet Supports the Open verification methodology for SystemVerilog.

VIP includes all functionality in verification to make the VIP more powerful. The monitor is used to track the bus traffic. It generates the log file to support the designers in verifying the Design.

The protocol checker dynamically checks for protocol violations and reports errors. Various rules are implemented for checking the behavior model.

The Perfectus VIP for Ethernet includes the following: Generator, BFM, Monitor, Checker, Coverage, and Scoreboard.

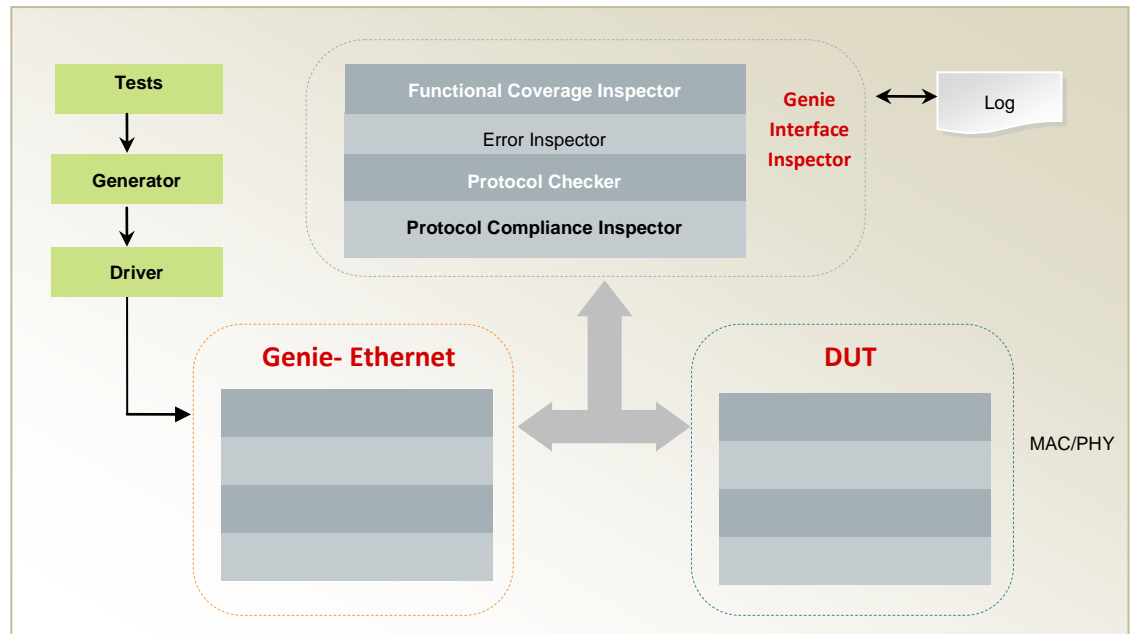


Figure 1: Block Diagram

Benefits

- Enables faster test bench development and more complete verification of Ethernet designs
- Simplifies results analysis
- Plug-and-play in every major simulation environment
- Enables self-checking test bench methodologies

Features	
<ul style="list-style-type: none"> Compliant to IEEE Std 802.3™ Specification, IEEE Std 802.3ba draft 	<ul style="list-style-type: none"> Supports ports capable of half duplex mode and full Duplex mode
<ul style="list-style-type: none"> Supports the management interface for all supported interfaces. Station management registers can be accessed both via MDIO interface and through test interface 	<ul style="list-style-type: none"> Simulates single or multiple Ethernet devices on a medium, generating and collecting Ethernet packets
<ul style="list-style-type: none"> Supports MII, GMII, XGMII, XLGMII, CGMII interfaces 	<ul style="list-style-type: none"> Includes protocol-based scenario generation
<ul style="list-style-type: none"> User can control configuration and generation of transactions for each device model. Supports configuration of different ports independently (Switch configuration for example, 1Gbps and 100 Mbps port in one switch) 	<ul style="list-style-type: none"> Fully configurable error generation (protocol errors and packet errors) allows testing of error detection mechanisms under realistic scenarios
<ul style="list-style-type: none"> Monitors protocol and reports violations 	<ul style="list-style-type: none"> Extensible coverage collection
<ul style="list-style-type: none"> Supports the frame types-MAC data, Control Pause, VLAN tagging 	<ul style="list-style-type: none"> Score boarding hooks provided along with simple generic homogeneous scoreboard
<ul style="list-style-type: none"> Configurable log file production (for datapath and station management) with test statistics. Comprehensive mechanism for trace/debug of VIP behavior 	<ul style="list-style-type: none"> Provision of extensive scenario generator library for user to develop advance scenarios for each interface
<ul style="list-style-type: none"> Major simulator support 	<ul style="list-style-type: none"> Full CSMA/CD support
<ul style="list-style-type: none"> Comprehensive documentation and support 	<ul style="list-style-type: none"> Configurable No of MACs and PHYs
<ul style="list-style-type: none"> Configurable enabling of Checker, Scoreboard, Coverage modules 	<ul style="list-style-type: none"> Configurable reset (Posedge or Negedge), Configurable enable of reset
<ul style="list-style-type: none"> Generation of random Interpacket gap 	<ul style="list-style-type: none"> Automatic generation of crc and padding
<ul style="list-style-type: none"> Configurable subtype MAC and PHY 	<ul style="list-style-type: none"> Configurable BFM modes: ACTIVE and PASSIVE
<ul style="list-style-type: none"> Simple yet extremely powerful test interface allows control over all aspects of VIP behavior and promotes re-use of test code 	

Deliverables	About Perfectus VIP	TestBench Language
<ul style="list-style-type: none"> Fully configurable VIP Sample test covering basic functionality User Guide & release notes 	<p>Perfectus other Verification IP includes:</p> <ul style="list-style-type: none"> USB 3.0 PCI Express 2.0 USB 2.0 SAS SATA Fibre Channel AMBA: - AHB, APB & AXI OCP SM bus FBDIMM 	<ul style="list-style-type: none"> Verification Environment is in SystemVerilog(OVM), for more controlled test bench scenarios