

# Genie ONFi 2.1 Verification IP

**Genie ONFi VIP** is compliant to ONFi 2.1 Revision specifications. It is a complete verification suite that helps designer to verify a NAND Flash Device. The VIP can behave as an ONFi Host and Transfer Command, Address and Data to NAND Flash Device according to configurations.

ONFi Interface Inspector used for protocol checking and debugging purposes. The ONFi Interface Inspector will monitor data transfer between ONFi Host & NAND Flash Device. It will Inspect Host /Device Features through Feature Inspector, It will inspect PIN/Timing Rules of Data Transaction in Protocol Compliance Inspector, Error Inspector will report Error incase of any violations in Rules & Functionality Coverage Inspector will inspect how much area & Functionality in NAND Flash Device covered.

ONFi Interface inspector will give functional coverage report & log info at the end of simulations.

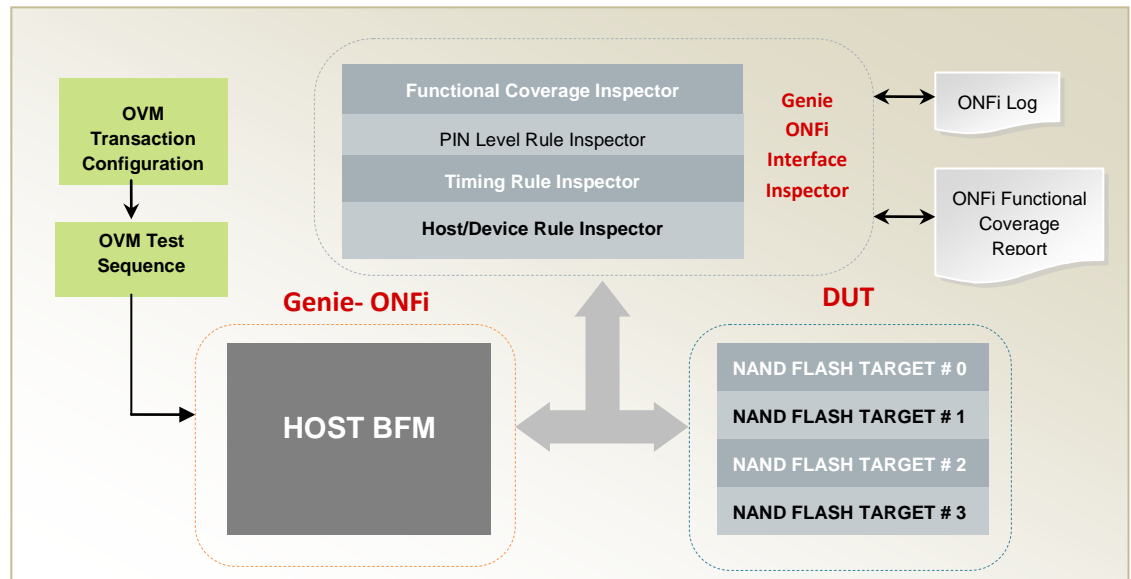


Figure 1: Genie- ONFi Block Diagram

## Features

<ul style="list-style-type: none"> <li>Fully compliant to the ONFi 2.1</li> </ul>	<ul style="list-style-type: none"> <li>Based on OVM 2.0</li> </ul>
<ul style="list-style-type: none"> <li>Supports Source Synchronous &amp; Asynchronous Mode of operations for individual Target Flash with all timing modes</li> </ul>	<ul style="list-style-type: none"> <li>Supports up to 4 Target NAND Flash Device with unlimited LOGICAL UNIT, BLOCK &amp; PAGE</li> </ul>
<ul style="list-style-type: none"> <li>Supports Interleaving READ Command Operations</li> </ul>	<ul style="list-style-type: none"> <li>Supports Partial Page Program Operations</li> </ul>
<ul style="list-style-type: none"> <li>Supports Multiple LUN Operations</li> </ul>	<ul style="list-style-type: none"> <li>Supports parallel command operation on dual bus</li> </ul>
<ul style="list-style-type: none"> <li>Supports 16 bit bus width operations</li> </ul>	<ul style="list-style-type: none"> <li>Supports Interleaving Command operations</li> </ul>
<ul style="list-style-type: none"> <li>Supports Clock stop feature during Source Synchronous mode of operations</li> </ul>	<ul style="list-style-type: none"> <li>Device Defective Operation sequence for each Target NAND Flash DUT</li> </ul>
<ul style="list-style-type: none"> <li>Supports Data Pause between Read/Program Operations</li> </ul>	<ul style="list-style-type: none"> <li>Supports Small Data Move command Operations</li> </ul>
<ul style="list-style-type: none"> <li>Supports Change ROW Address Command Operations</li> </ul>	<ul style="list-style-type: none"> <li>Ability to generate Vendor Specific Commands</li> </ul>
<ul style="list-style-type: none"> <li>Automatic/Device/User Configured Timing &amp; feature Parameters for each Target Flash Device</li> </ul>	<ul style="list-style-type: none"> <li>APIs to generate User Configurable Transactions, to generate User Configurable Set of Transactions to cover large area of Device, to generate User Configurable Error Transactions</li> </ul>
<ul style="list-style-type: none"> <li>Test Suite covers all type of functional scenarios, all Error scenarios</li> </ul>	<ul style="list-style-type: none"> <li>Functional Coverage Report for all attached Target NAND Flash device</li> </ul>

## Product Details

Genie - ONFi VIP Consist of following modules:

**ONFi SEQUENCER:** Supports Random Sequence generation & arbitrations given in test sequence.

**ONFi HOST DRIVER:** Drive Generated Sequence to NAND Flash Device DUT according to configured Timing Parameters & Features.

**ONFi MONITOR:** Receive Response from NAND Flash Device DUT and Perform Data Integrity check & Functional Coverage.

**ONFi INTERFACE INSPECTOR:** Verify all Rules of Protocol & Timing on Interface run time.

Benefits	
<ul style="list-style-type: none"> <li>▪ OVM 2.0 based System Verilog source code</li> </ul>	<ul style="list-style-type: none"> <li>▪ TLM Based Architecture of BFM &amp; Test bench</li> </ul>
<ul style="list-style-type: none"> <li>▪ OVM Test Sequence for test case</li> </ul>	<ul style="list-style-type: none"> <li>▪ Error Injections any where in transaction</li> </ul>
<ul style="list-style-type: none"> <li>▪ Command &amp; Functional API to Automate Generations of transactions.</li> </ul>	<ul style="list-style-type: none"> <li>▪ Perform Functional Coverage for all attached NAND Flash Target Device individually</li> </ul>
<ul style="list-style-type: none"> <li>▪ Test suit available for all type of transactions</li> </ul>	<ul style="list-style-type: none"> <li>▪ Detailed LOG Report for Easy Debug</li> </ul>
<ul style="list-style-type: none"> <li>▪ Configurable Verbosity Level for LOG Generations</li> </ul>	<ul style="list-style-type: none"> <li>▪ Run Time Configurable Parameters of all Features &amp; Timing Mode</li> </ul>

Supported Platform	About Perfectus VIP	Support & Training
Windows, Linux , Solaris	Perfectus other Verification IP includes: <ul style="list-style-type: none"> <li>▪ USB 3.0</li> <li>▪ SAS</li> <li>▪ SATA</li> <li>▪ AMBA: - AHB, APB &amp; AXI</li> <li>▪ OCP</li> <li>▪ Fibre Channel</li> <li>▪ AMB</li> <li>▪ SM bus</li> <li>▪ FBDIMM</li> <li>▪ PCI-Express</li> <li>▪ SPI 4.2</li> <li>▪ Ethernet 100Mbps/1G/10G</li> <li>▪ USB 2.0</li> </ul>	<ul style="list-style-type: none"> <li>▪ Fast bug fixing</li> <li>▪ Online support service</li> <li>▪ On demand training</li> </ul>
Supported Simulators		Perfectus Verification IP support the various environments <ul style="list-style-type: none"> <li>▪ SystemC &amp; SystemVerilog</li> <li>▪ Verilog HDL &amp; VHDL</li> <li>▪ C/C++</li> <li>▪ Vera &amp; e</li> </ul>
Modelsim , NCSIM , VCS		
Deliverables		
<ul style="list-style-type: none"> <li>▪ Fully configurable BFM</li> <li>▪ Sample test &amp; Extensive tests covering basic functionality</li> <li>▪ User Guide &amp; release notes</li> </ul>		