

## Verification IP

**GENIE-SSU VIP** is compliant to Super Speed USB3.0 specifications. It is a complete verification suite that helps designer to verify a USB 3.0 based designs. The VIP can behave as a host (or a downstream port entity) or it can behave as a device (or an upstream port entity) based on the configuration of the VIP. Genie-SSU ships with a **Compliance Suite** consisting of 400+ tests which ensures robust verification, maximum functional and feature coverage

**SSU Interface-Inspector** and Monitor are used for protocol checking and debugging purposes. SSU Interface-Inspector, has a further hierarchical division of link layer and protocol layer to do the checks pertaining to the corresponding layers, which operates at the bus (are connected to the Tx and Rx lines of the USB bus defined for USB 3.0) and thus can be efficiently used with any environment configuration.

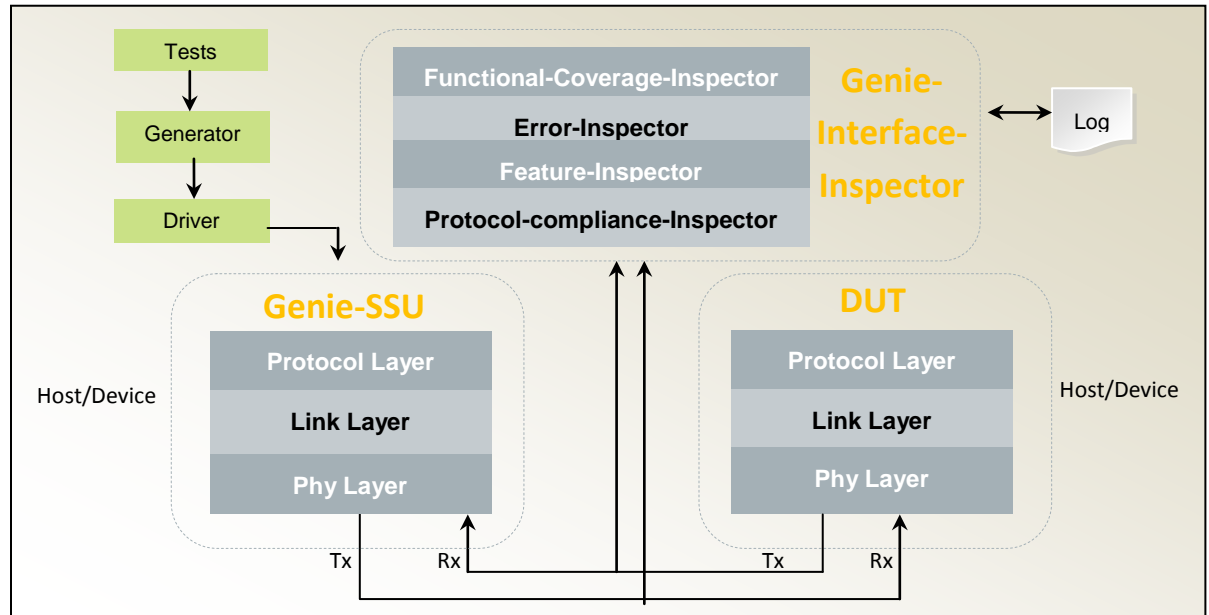


Figure 1: Block diagram

### Features

<ul style="list-style-type: none"> <li>Fully compliant to the Super Speed USB 3.0</li> </ul>	<ul style="list-style-type: none"> <li>Configurable for 0 to 15 endpoints</li> </ul>
<ul style="list-style-type: none"> <li>Automatic handling of Protocol Link and physical layer packets.</li> </ul>	<ul style="list-style-type: none"> <li>Automatic /user configurable generation of flow control packets</li> </ul>
<ul style="list-style-type: none"> <li>Full LTSSM (Link Training &amp; Status State Machine)</li> </ul>	<ul style="list-style-type: none"> <li>Configurable packet size for data packet payloads</li> </ul>
<ul style="list-style-type: none"> <li>Automatic /user configurable generation of isochronous time stamp packets ( for host configuration )</li> </ul>	<ul style="list-style-type: none"> <li>Supports Randomization for packet fields and data payload with or without error injection</li> </ul>
<ul style="list-style-type: none"> <li>Configurable TS1, TS2 , TSEQ ,SKP Ordered set generation</li> </ul>	<ul style="list-style-type: none"> <li>Generation of packets directed for hubs also supported</li> </ul>
<ul style="list-style-type: none"> <li>Automatic /user configurable generation of all LMP packets ( for both host and device configurations of the VIP )</li> </ul>	<ul style="list-style-type: none"> <li>Supports Power Management :                             <ol style="list-style-type: none"> <li>Low power mode enable/disable (U1/U2)</li> <li>Suspend (U3)</li> <li>Active state (U0).</li> <li>Resume/Remote Wakeup</li> </ol> </li> </ul>
<ul style="list-style-type: none"> <li>Supports all 4 kinds of transactions ( control , isochronous , interrupt and bulk )</li> </ul>	<ul style="list-style-type: none"> <li>Supports LFPS signal generation and detection</li> </ul>
<ul style="list-style-type: none"> <li>Support for generation of all link commands defined in the USB 3.0 specification</li> </ul>	<ul style="list-style-type: none"> <li>Supports generation/storing of Hub specific descriptors</li> </ul>
<ul style="list-style-type: none"> <li>Supports generation LMP packets for Hub.</li> </ul>	<ul style="list-style-type: none"> <li>Supports Loopback</li> </ul>
<ul style="list-style-type: none"> <li>Supports Data transactions to device connected on Hub</li> </ul>	<ul style="list-style-type: none"> <li>Supports Control transaction specific to Hub</li> </ul>

# Product Details

GENIE SSU VIP consists of the following modules:

**SSU HOST:** Supports packets generation as a Super Speed host. The Responses of the host can be automated or can be controlled by the user.

**SSU DEVICE:** The BFM can respond to the transactions generated by the host or can behave in a user defined way (useful for error injection scenarios).

**SSU Monitor:** SU monitor generates formatted LOG file and tracks the traffic of the bus which makes debugging easier.

**SSU Interface-Inspector:** SSU Interface-Inspector provides protocol-checking capability. Checks are configurable. They can be enabled and disabled individually for a particular test. Various verbosity levels are supported for warning, debug, errors and log.

## Benefits

<ul style="list-style-type: none"> <li>System Verilog source code for BFMs and test-cases</li> </ul>	<ul style="list-style-type: none"> <li>Inject errors at all layers</li> </ul>
<ul style="list-style-type: none"> <li>Complete set of fully functional BFM and test-benches for USB 3.0 components: host Device</li> </ul>	<ul style="list-style-type: none"> <li>Tests are self-checking, portable, and reusable on most types of designs</li> </ul>
<ul style="list-style-type: none"> <li>Robust BFM APIs automate sending TPs/DPs, controlling automatic BFM device response behavior and link state transitions</li> </ul>	<ul style="list-style-type: none"> <li>Test suites include Perfectus-based host, device test-suites (which contain basic , random, user defined tests ) that target high compliance coverage from their corresponding checklists</li> </ul>

### Test Bench

Test case files are of the following types in Environment

- System Verilog - For more controlled test bench scenarios

### Supported Platform

Windows, Linux , Solaris

### Supported Simulators

Modelsim , NCSIM , VCS

### Deliverables

- Fully configurable BFM
- Sample test & Extensive tests covering basic functionality
- User Guide & release notes

### About Perfectus VIP

- Perfectus other Verification IP includes:
- SAS
  - SATA
  - AMBA: - AHB, APB & AXI
  - OCF
  - Fibre Channel
  - AMB
  - SM bus
  - FBDIMM
  - PCI-Express
  - SPI 4.2
  - Ethernet 100Mbps/1G/10G
  - USB 2.0
  - ONFI

Perfectus Verification IP support the various environments

- SystemC & SystemVerilog
- Verilog HDL & VHDL
- C/C++
- Vera & e

### Support & Training

- Fast bug fixing
- Online support service
- On demand training

### Example Topologies

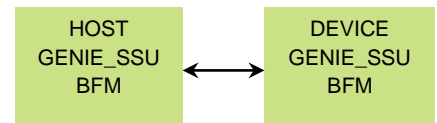


Figure 2: Example01

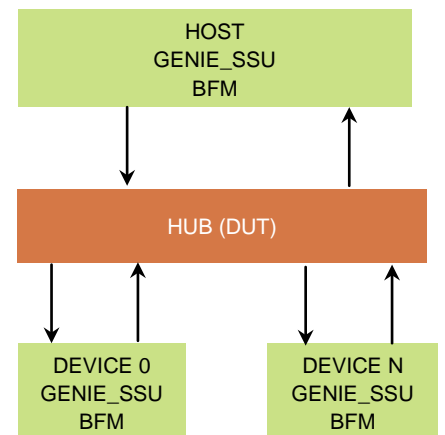


Figure 3: Example02