

Verification IP SPI 4.2

The **Perfectus VIP for SPI 4.2** provides an efficient algorithm to verify the SPI based designs by giving the advance techniques including the support for System Verilog assertions.

The VIP comprised of BASIC TEST to verify the BFM. It also includes COMPLIANCE and RANDOM TESTING to make the VIP more powerful. The monitor is used to track the bus traffic. It generates the LOG file to support the designers in verifying the VIP. The Checker is used for bug fixing inside the BFM. Various rules are implemented for checking the behavior model. The Perfectus VIP for SPI includes the following:- SPI BFM , SPI monitor and Checker. The Perfectus VIP also includes supports for System Verilog assertions which includes following:

- Functional assertions
- Timing assertions
- State Machine assertions

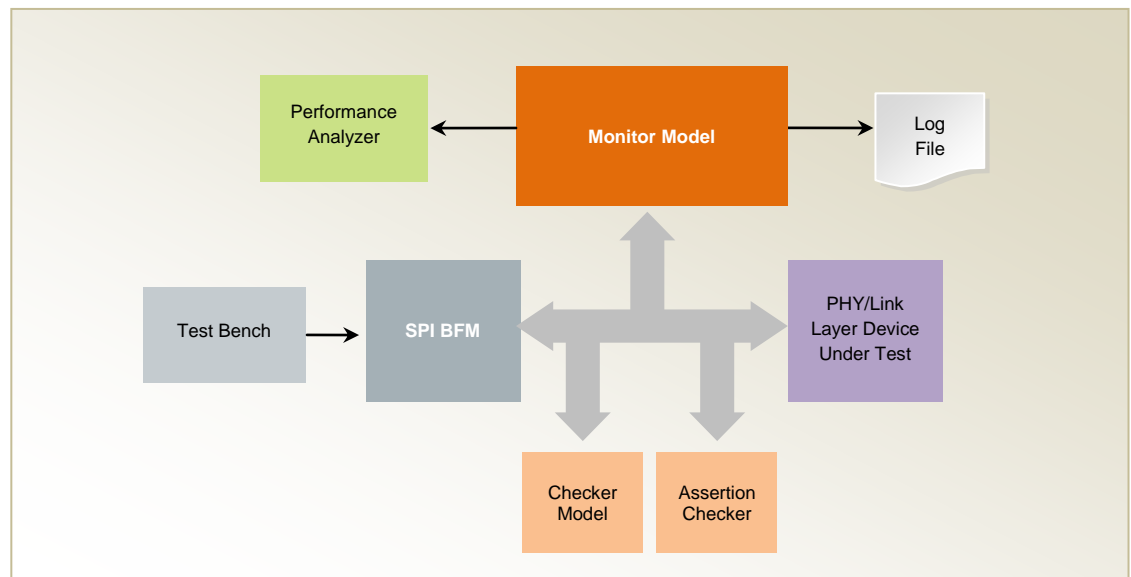


Figure 1: VIP for SPI system

Features

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|---|---|
| ▪ Configurable datapath width (32 bits, 64 bits, 128 bits) | ▪ FIFO buffer status management and indications |
| ▪ Conforms to Optical Internetworking Forum specification OIFSPI4-02.0 System Packet Interface Level 4 Phase 2 standard | ▪ Supports up to 256 Asymmetric ports and calendar lengths up to 1024, allowing for uneven bandwidth allocation across channels |
| ▪ Error detection and handling | ▪ Configurable training patterns |
| ▪ Flexible start of packet (SOP) alignment to a byte lane | ▪ Run-time programmable calendar length, burst size, and threshold levels |
| ▪ Bus Arbitration Scheme with channel fairness - user programmable weighting and length | ▪ Allows for per-port configurable maxburst values creating maximum flexibility |
| ▪ Supports dynamic bit de-skew over full frequency range | |

Product Details

SPI BFM: The SPI-4 protocol is an interface with a physical layer device on one side and a link layer device on the other side. Both devices can initiate data transfer and send FIFO status and also, the both devices can receive FIFO status information and data sent from the other device.

Suitable for verification in a wide range of SPI-4.2 applications

- Channeled Physical Layer Framers
- Bridge Chips
- Network Processors
- Traffic Managers

SPI MONITOR: SPI monitor generates LOG file and tracks the traffic of the bus. User configurable LOG file. Programmable file names for logging information. Also supports Performance Analysis and Functional Coverage.

SPI CHECKER: SPI checker provides bus-level protocol checking capability. It performs real-time reporting of errors on the clock in which the End symbol of a packet is received.

Benefits

- | | |
|---|--|
| ▪ Configurable and easy to use | ▪ Simplifies design verification process |
| ▪ BFM commands are fully user configurable. | ▪ Reduces development costs |
| ▪ Faster Test bench development and supports RANDOM and COMPLIANCE Test cases | ▪ Speeds time-to-market with new SoCs |

Supported Platform

Windows, Linux

Supported Simulators

VCS 7.x, NCVerilog 5.x, Modelsim 6.x

Deliverables

- Fully configurable BFM
- Sample test & Extensive tests covering basic functionality
- User Guide, Assertion Document & release notes

About Perfectus VIP

Perfectus other Verification IP includes:

- SAS
- SATA
- AMBA: - AHB, APB & AXI
- OCP
- Fibre Channel
- AMB
- SM bus
- FBDIMM

Test Bench Language

Test case files are of two types in Environment:

- Text - *Simple file controlling the knob.*
- Verilog - *For more controlled test bench scenarios*

Support & Training

- Fast bug fixing
- Online support service
- On demand training

Perfectus Verification IP support the various environments

- SystemC & SystemVerilog
- Verilog HDL & VHDL
- C/C++
- Vera & e