



Data Sheet

Perfectus Verification IP OCP Interface

Overview

The Perfectus VIP for OCP provides an efficient bus-independent interface between IP cores that reduces design time, design risk, and manufacturing costs for SOC designs that support Verilog HDL assertions.

The VIP comprised of BASIC TEST and COMPLEX TEST to verify the Design. It also includes all functionality in TESTING to make the VIP more powerful. The monitor is used to track the bus traffic and also for monitoring in both master and slave side. It generates the LOG file to support the designers in verifying the Design.

The protocol checker dynamically checks for protocol violations and reports errors. Various rules are implemented for checking the behavior model.

The Perfectus VIP for OCP includes the following: - OCP master, OCP slave, OCP monitor and OCP protocol checker.

Features

- Small Set of Mandatory signals and large set of optional signals.
- Synchronous, uni-directional signaling allows simplified implementation, integration.
- Configurable address and data word width.
- Transfers may be pipelined to any depth for increased throughput.

Benefits

- Supports back to back environment.
- Can be placed easily in any Soc Design.
- BFM commands are fully user configurable.
- Faster Test bench development and supports BASIC and RADOM Test cases.
- Executable in every major simulation environment.

Product Details

OCP Master: OCP master initiates transfer on the bus. User configurable knobs to support various features of master.

OCP Slave: The slave responds to commands presented to it, either by accepting data from the master, or presenting data to the master. It supports random assertion and de-assertion of SCmdAccept, SDataAccept.

OCP Monitor: OCP monitor generates LOG file and tracks the traffic of the bus.

OCP Checker: OCP checker provides protocol-checking capability. During checking, if any error occurs then it will finish the simulation.

TestBench Language: Test case files are of two types in Environment.

- Text - Simple file controlling the knobs.
- Verilog - For more controlled test bench scenarios.

Supported Platform: Windows, Linux.

Supported Simulators: VCS 7.x, NCVerilog 5.x, Modelsim 6.x.

Deliverables

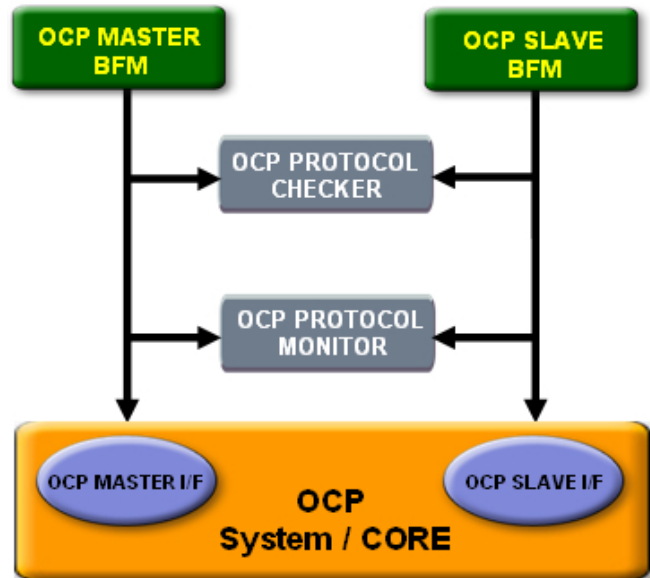
Perfectus deliverables includes:

- Fully configurable BFM
- Sample & Extensive tests covering basic functionality
- User Guide, Assertion Document & release notes

Support & Training

- Fast bug fixing
- Online support service
- On demand training

Block Diagram



VIP for OCP System

About Perfectus VIP

Perfectus other Verification IP includes:

- SAS
- SATA
- AMBA: - AHB, APB & AXI
- OCP
- Fibre Channel
- AMB
- SM bus
- FBDIMM

Perfectus Verification IP support the various environments

- SystemC & SystemVerilog
- Verilog HDL & VHDL
- C/C++
- Vera & e

For more information visit our site www.perfectus.com