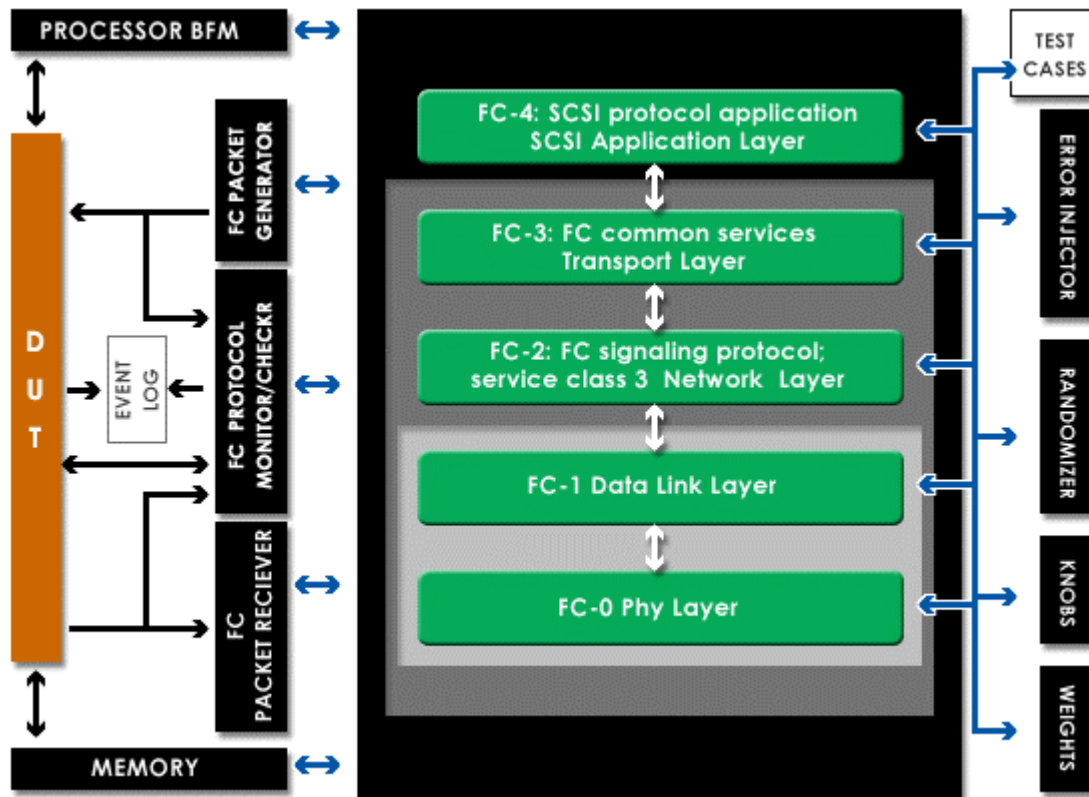


Verification IP Fiber Channel

Highlights:

- Complete Functional Verification Engine for test generation and FC protocol checking and monitoring
- FC Compliance Suite (>200 tests) compatible with FC-0, FC-1, FC-2, and FC-4) for verifying Initiators and Targets
- Verifies all protocol layers (FC-0, FC-1, FC-2, and FC-4)
- Directed and Randomized Test Generation
- Directed and Randomized Error Injection capability
- Callback functionality
- Programmable parameters through Knobs
- User configurable Test reports for logging events and transactions
- Interoperable with various Verification Environments like NC-Sim, Specman, VERA, VCS, ModelSim etc
- Selectable Pin Interface
- Supports link speeds 1G, 2G & 4G
- Multiple Language Interface like Verilog, VHDL, C/C++, SystemC, 'e', VERA, SystemVerilog

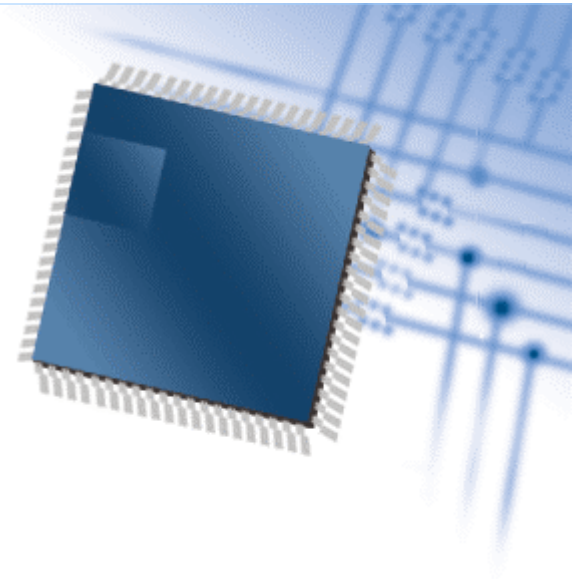
Figure 1: Block diagram



Genie-FC™ Solution

Perfectus has created a two-tiered product specifically aimed at delivering Fibre Channel controller designs to market faster, with reduced effort and higher quality. These products are designed to solve the problem that absorbs the largest resources, time, and has the highest risk of a design – the verification effort. These products are:

- Genie FC Verification Engine
- FC Sanmark Compliance Suite
- FC Assertions



Genie-FC™ Verification Engine

Genie FC Verification engine provides a quick and efficient way to verify ASIC or FPGA designs having a FC Interface. It supports generation of tests for all layers (FC-0, FC-1, FC-2, FC-3 and FC-4). The powerful FC controller can generate transactions from high-level commands embedded in the Engine to individual layers. As users automatically develop tests that generate transactions and respond to bus activity, they can inject errors at any point and depend on the FC Protocol Checkers to verify bus compliance of the DUT and the Report Generator to report any violation. This Engine enables higher productivity, performance and quality, resulting in higher confidence in verification results as well as reducing the verification process. The components of the FC Verification Engine are:

- Directed & Random tests generator
- Callback Functionality
- Error injector
- Report generator
- Frame / primitive generator
- Protocol checkers & Monitors
- FC Knob & Weights

Genie-FC™ Compliance suite

Developed by Perfectus to test proper working of FC devices, the compliance suite is a comprehensive verification test suite that provides dramatic resource and timesavings for verification of a FC design. These tests

have been created and continuously refined with multiple customer designs.

- Designed to the FC standards to secure your verification investments
- Provides Comprehensive design coverage with more than 200 self checking tests targeted at FC-0, FC-1, FC-2, FC-3 and FC-4 layers
- Reduces the Verification Effort (3 man months with the suite versus >48 man months without the compliance suite)
- Used by multiple customers to test actual designs
- Compliance suite runs on hardware emulation as well as in simulation
- Provides a (directed) random regression capability as well
- Most effective solution to find more bugs in less time
- >95% coverage

[Call for more details on Genie-FC™ Assertions](#)

Environment

- Verilog
- VHDL
- C++/C
- 'e'
- SystemC
- SystemVerilog
- VERA