

Data Sheet

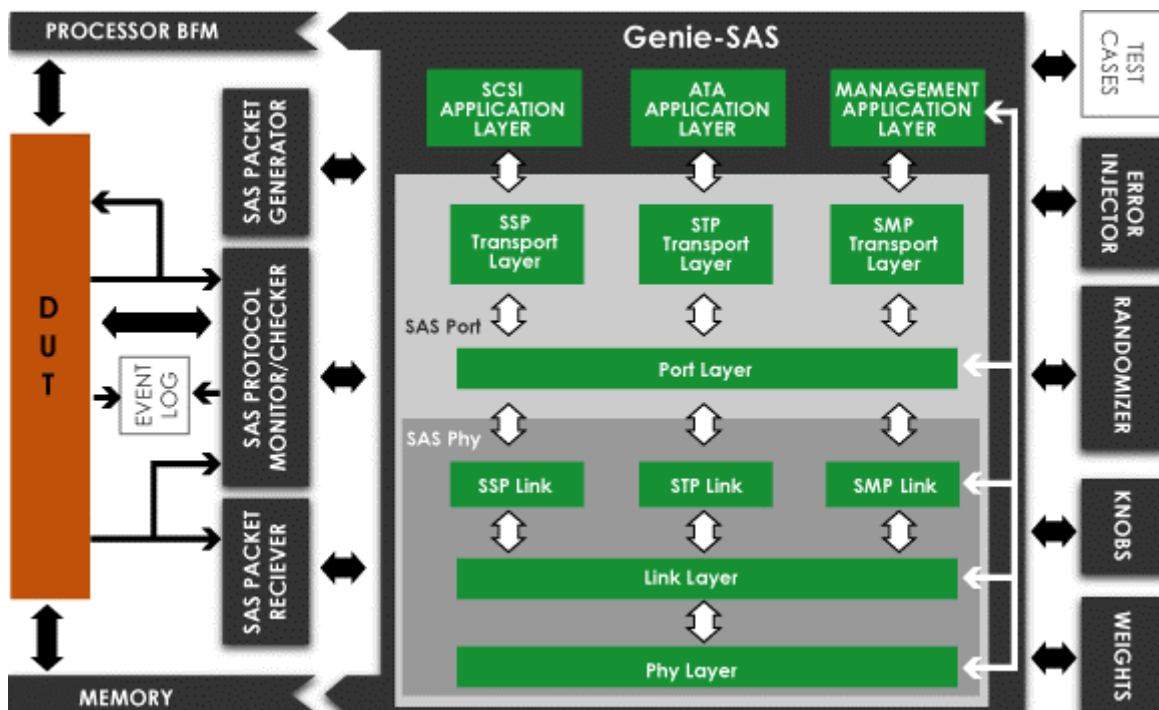
Genie-SAS™

Verification Engine, Assertions, Compliance Test Suite

Highlights

- Complete Functional Verification Engine for test generation and SAS protocol checking and monitoring
- SAS Compliance Suite (>200 tests) compatible with SAS-1.1 and SAS-2 for verifying Initiators and Targets
- Verifies all protocol layers (PHY, Link, Port, Transport and Application)
- Directed and Randomized Test Generation
- Directed and Randomized Error Injection capability
- Callback functionality
- Programmable parameters through Knobs
- Support for Various Link Speeds (1.5G, 3G and 6G)
- Wide Port Support
- User configurable Test reports for logging events and transactions
- Interoperable with various Verification Environments like NC-Sim, Specman, VERA, VCS, ModelSim etc
- Selectable Pin Interface
- Multiple Language Interface like Verilog, VHDL, C/C++, SystemC, 'e', VERA, SystemVerilog

Figure 1: Block diagram





Genie SAS™ Verification Engine

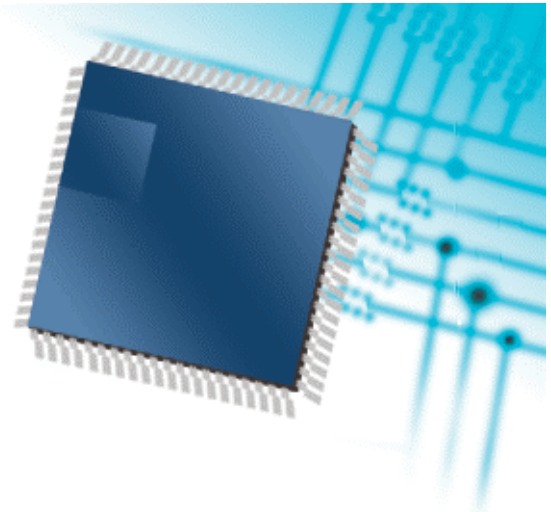
Genie SAS Verification engine provides a quick and efficient way to verify ASIC or FPGA designs having a SAS Interface. It supports generation of tests for all layers (Application, Transport, Port, Link and PHY). The powerful SAS controller can generate transactions from high-level commands embedded in the Engine to individual layers. As users automatically develop tests that generate transactions and respond to bus activity, they can inject errors at any point and depend on the SAS Protocol Checkers to verify bus compliance of the DUT and the Report Generator to report any violation. This Engine enables higher productivity, performance and quality, resulting in higher confidence in verification results as well as reducing the verification process. The components of the SAS Verification Engine are:

- Directed & Random tests generator
- Callback Functionality
- Error injector
- Report generator
- Frame / primitive generator
- Protocol checker
- SAS controller

Perfectus SAS Compliance suite

Developed by Perfectus to test proper working of SAS devices, the compliance suite is a comprehensive verification test suite that provides dramatic resource and time saving for verification of a SAS design. These tests have been created and continuously refined with multiple customer designs.

- Designed to the SAS standards to secure your verification investments
- Provides Comprehensive design coverage with more than 200 self checking tests targeted at OOB, Link, Transport & Command layer
- Reduces the Verification Effort (3 man months with the suite versus >48 man months without the compliance suite)
- Used by multiple customers to test actual designs



- Compliance suite runs on hardware emulation as well as in simulation
- Provides a (directed) random regression capability as well
- More bugs in less time with >95% coverage

SAS Assertions

SAS SystemVerilog Assertion Suite is fully compliant to SATA-Revision 2.0. SAS protocol checks are implemented as SVA properties. Following are the main property sets:

- State Transitions, Watch-Dog Timer and various Timeouts
- Phy Layer OOB Detection, State Machines, Speed Negotiation.
- 8b/10b Decoding / Encoding, Primitive Decoding / Encoding / Sequencing
- Link Layer State Machines and Link Layer Sequences.
- Transport Layer State Transitions, Frame Generator / Assembler, CRC checker
- Command Layer State Machine, Command-Response Sequences.

Environment

- Verilog
- VHDL,
- C++/C
- 'e'
- SystemC,
- SystemVerilog
- VERA