

Data Sheet

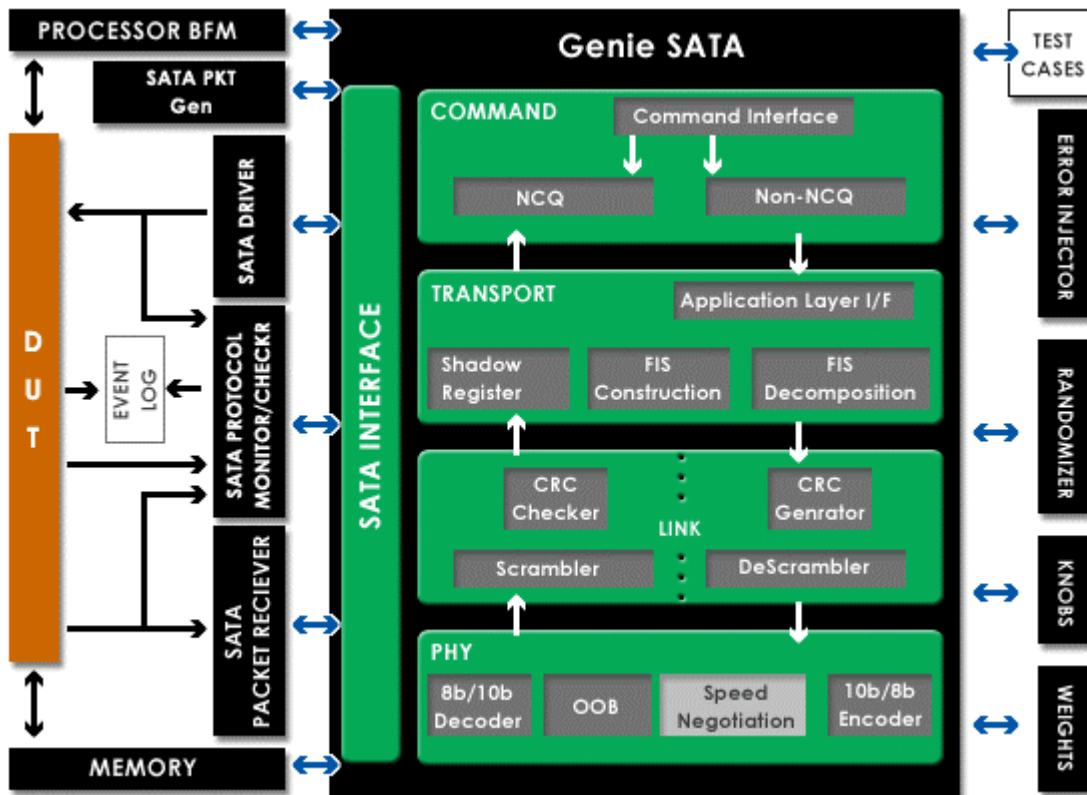
Genie-SATA™

Verification Engine, Compliance Test Suite, Assertions, & FPGA Board

Highlights:

- Complete Functional Verification Engine for test generation and SATA protocol checking and monitoring
- SATA Compliance Suite (>200 tests) compatible with SATA-I and SATA-II for verifying Initiators and Targets
- Verifies all protocol layers (PHY, Link, Transport and Command)
- Directed and Randomized Test Generation
- Directed and Randomized Error Injection capability
- Callback functionality
- Programmable parameters through Knobs
- Support for Link Speeds (1.5G, 3G)
- NCO and Port Selector Support
- User configurable Test reports for logging events and transactions
- Interoperable with various Verification Environments like NC-Sim, Specman, VERA, VCS, ModelSim etc
- Selectable Pin Interface
- Multiple Language Interface like Verilog, VHDL, C/C++, SystemC, 'e', VERA, SystemVerilog

Figure 1: Block diagram





Genie SATA™ Verification Engine

SATA BFM supports generation of tests for all layers (Command, Transport, Link and PHY). As users automatically develop tests that generate transactions and respond to bus activity, they can inject errors at any point and depend on the SATA Protocol Checkers to verify bus compliance of the DUT and the Report Generator to report any violation. The components of the SATA Verification Engine are:

- Directed & Random tests generator
- Callback Functionality
- Error injector
- Report generator
- Frame/primitive generator
- Protocol Checker
- Protocol Monitor

SATA Compliance suite

The compliance suite is a comprehensive verification test suite that provides dramatic resource and time saving for verification of a SATA design.

- Provides Comprehensive design coverage with more than 200 self checking tests targeted at OOB, Link, Transport & Command layer
- Reduces the Verification Effort (3 man months versus 48 man months)
- Used by multiple customers to test actual designs
- Runs also on hardware emulation
- Provides a constrained random regression capability using Knob Files
- More bugs in less time with >95% coverage

SATA FPGA Board

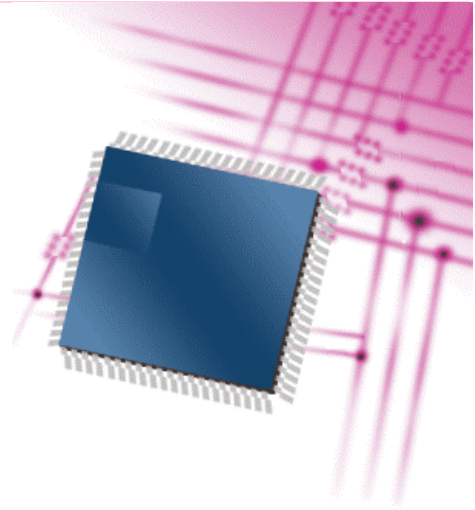
Created with SATA development in mind, the board provides the user with up to 3 to 6 million gates using high-speed FPGA devices. Optional connectors allow the addition of external SRAM, SDRAM, user-specific micro controller cards (ARM, MIPS, PowerPC, etc), a general-purpose interface adapter slot, and a Serial ATA PHY card. Perfectus supplies all of these components plus a GUI-based applications/control program to drive the board from a host (Windows 2000-based) workstation. The other benefits the board provides are:

- Enable early Firmware development capability
- Increased verification cycles
- Verify design with industry standard devices
- Reduced chances of functional and logic bugs
- Allows lab debug of silicon devices
- Allows characterization of silicon Low cost compared to other hardware emulation or verification systems

SATA Assertions

SATA SystemVerilog Assertion Suite is fully compliant to SATA-Revision 2.0. SATA protocol checks are implemented as SVA properties. Following are the main property sets:

- State Transitions, Watch-Dog Timer and various Timeouts
- Phy Layer OOB Detection, State Machines, Speed Negotiation.
- 8b/10b Decoding / Encoding, Primitive



Decoding / Encoding / Sequencing

- Link Layer State Machines and Link Layer Sequences.
- Transport Layer State Transitions, Frame Generator / Assembler, CRC checker
- Command Layer State Machine, Command-Response Sequences.

Environment

Verilog, VHDL, C++/C, 'e', SystemC, SystemVerilog, VERA

Other Perfectus VIPs

Perfectus other Verification IP includes:

- SAS
- SATA
- AMBA: AHB, APB & AXI
- OCP
- Fibre Channel
- AMB
- SM bus
- FBDIMM