

DATA SHEET

# PCI Express 2.0

## Genie-PCIe™ Verification IP

### Overview

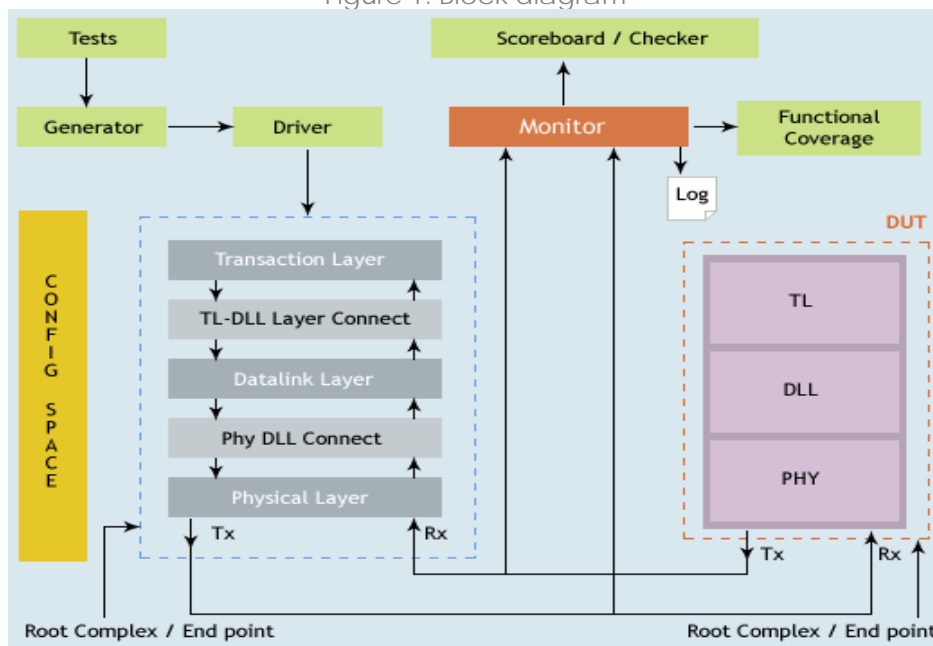
Genie-PCIe provides robust verification of PCI Express based designs that reduces design time, design risk, and costs for verification. Verification-IP provides functional behavior defined under PCI Express Base Specification 2.0 and is also backward compatible with PCI Express Base Specification 1.1 and 1.0a.

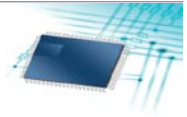
It comes equipped with BFM, which can be configured as both Root Complex and Endpoint, Protocol Monitor (Independent entity) and a Protocol checker laden with 300+ Protocol checking rules.

Genie-PCIe ships with Compliance Test suite based on list by PCI-SIG and 1500+ testcases which enables robust and easy verification.

Genie-PCI Express verification component granularity in system Architecture is at port level and hence one instance of this component means one port. The Verification IP is highly configurable and supports PHY connection with PIPE (PHY Interface for PCI Express Architecture) version 1.87 and standard serial configuration. Verification-IP is written in native SystemVerilog language.

Figure 1: Block diagram





## Single-link operation:

In the single-link mode, BFM is configured as a single link supporting x1, x2, x4, x8, x12, x16 or x32 operation.

## RC and EP operation:

In the single-link mode, the BFM can be configured as an Endpoint or Root Complex. BFM is enriched with Knobs to provide complete configurability over packet transmission and reception behavior. Simple and easy APIs allow user to inject packets/errors at any layer level.

## PCIe Monitor:

PCIe monitor generates LOG file and tracks the traffic of the link and display protocol specific transmission of packet information. Verbosity level of logs can individually be set by the user. Monitor log file can be tailored by the user depending on the requirement.

## PCIe Checker:

PCIe checker provides protocol-checking capability with following in-built rules:

- Endpoint rules
- Root Complex Integrated Endpoint Rules
- TLPs with Data Payloads – Rules
- Routing and Addressing Rules
- First/Last DW Byte Enables Rules
- Memory, I/O & Configuration Request Rules
- Message Request Rules
- Completion Rules
- Request Handling Rules
- Completion Handling Rules
- Transaction Ordering Rules

## TestBench Language:

Testcase files in Environment is of the following type:

- System Verilog - For more controlled test bench scenarios.

## Supported Platform:

Windows, Linux and Solaris

## Supported Simulators:

VCS 7.x,NCVerilog 5.x, Modelsim 6.x

## About Perfectus

### Perfectus other

#### Verification IP includes :

- SAS 2.0
- SATA - II
- AMBA :- AXI,APB, AHB
- OCP
- USB 2.0, 3.0
- SPI 4.2
- Fibre Channel
- Ethernet 1G/10G
- SMBus 2.0

### Perfectus Verification

#### IP support the various environments:

- System C
- System Verilog
- Verilog HDL
- VHDL
- C/C++
- Vera
- e

## Features

- Compliant with PCI Express Specification v1.0a, v1.1 and v2.0.
- Verification IP configurable as both Root complex and Endpoint
- Verification at PIPE, 10b, and serial interface.
- Complete Configurable Order Management logic
- Link width support: x1, x2, x4, x8, x12, x16, x32
- Polarity inversion
- 8-bit or 16-bit PIPE support
- Automatic/User configurable handling of all Layer packets
- Up to 8 virtual channels
- Full LTSSM (Link Training & Status)
- Automatic/User configurable generation of flow control packets , credit management
- Provides read and write transfers to memory, I/O, and configuration space
- Supports Error Injection at all layers.
- Test suites include the PCI-SIG-based compliance tests in addition to test-suites that target high compliance coverage from their corresponding checklists.
- Generates block read and write transfers to memory space and message transfers

## Benefits

- System Verilog source code format for BFM's and test-cases.
- Complete set of BFM's and test-cases for PCI Express component: Endpoint, Root Complex.
- Robust BFM API automates sending TLPs/DLLPs and controlling automatic BFM device response behavior and link and device state transitions.
- Supports transaction-oriented request-completion and error injection sequences based on address and command type attributes.