



Data Sheet

Perfectus Design IP

SMBus

Overview

Perfectus DIP for SMBus provides an efficient way to integrate SMBus Controller in the SOC or any Chip design utilizing SMBus Interface.

SMBus is a derivative of the I2C bus and is a serial, two-wire interface used in many rechargeable (secondary) battery systems because of its low overhead. The two-wire interface minimizes interconnections so ICs have fewer pins, and the number of traces required on printed circuit boards is reduced. Capable of 100 KHz operation, each device connected to the bus is software addressable by a unique address with a simple Master protocol. SMBus Controller design contains a synchronous interface and provides SMBus Master capabilities.

Features

- Compliant to SMBus 2.0 specification
- Generates and drives bus traffic as a SMBus 2.0 Requester
- The Design can be customized easily to meet any SOC needs
- The implementation of the SMBus Controller supports the following features:
 - Input Handler interface (A simple read/write interface supporting 32bit operation)
 - Master operation
 - Multi-master operation
 - Software selectable acknowledge bit
 - Arbitration lost signal
 - START and STOP signal generation
 - Repeated START signal generation
 - Acknowledge bit generation/detection
 - Bus busy detection
 - 100 KHz operation
 - Fully programmable COMMAND Encoding
 - PEC insertion
 - PEC error detection
 - SMBus Interface Idle detection
 - NACK error detection
 - TLOW error detection (Condition where Slave extends TLOW beyond the stipulated time)
 - Fully Programmable SMBCLK generation
 - PEC enable/disable control
 - Fully programmable Retry for NACKed transaction with a Retry buffer
 - Software controlled RESET implementation
 - Fully programmable Slave addressing

Product Details

SMBus Master: SMBus master initiates transfer on the bus. SMBus Master is capable to support any, including the following Transfer types:

- Byte Read/Write with/without PEC
- Word Read/Write with/without PEC
- Block Read/Write with/without PEC
- Process Call
- Quick Command

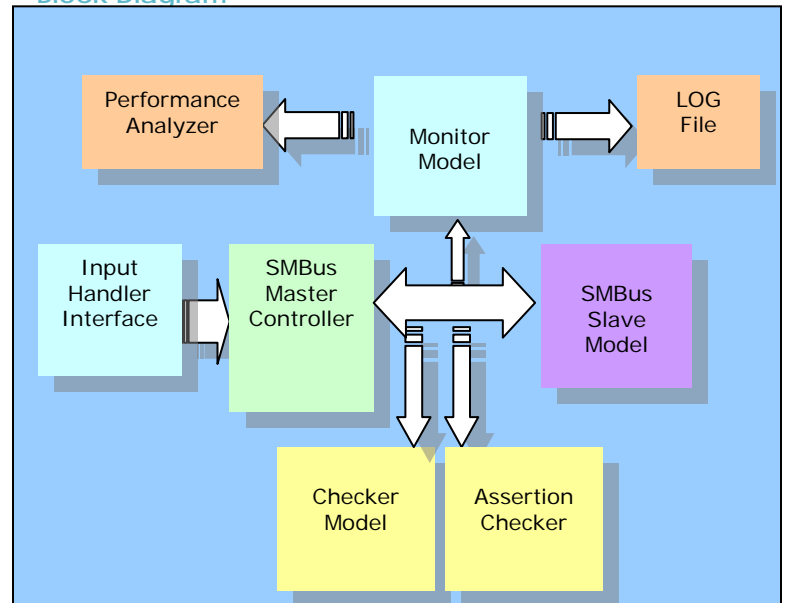
Benefits

- Can be easily placed in any Soc Design.
- Optimal design for Fast Internal clocking upto 200 Mhz

Supported Platform: Windows, Linux.

Supported Simulators: VCS 7.x, NCVerilog 5.x, Modelsim 6.x.

Block Diagram



Deliverables

Perfectus deliverables includes:

- SMBus Master Controller RTL/Netlist/GDSII netlist

Support & Training

- Fast bug fixing
- Online support service
- On demand training

Perfectus Verification IP includes:

- SAS
- SATA
- AMBA: - AHB, APB & AXI
- OCP
- Fibre Channel
- AMB
- SM bus
- FBDIMM

Perfectus Verification IP support the various environments

- SystemC & SystemVerilog
- Verilog HDL & VHDL
- C/C++
- Vera & e

For more information visit our site
www.perfectus.com