

Data Sheet

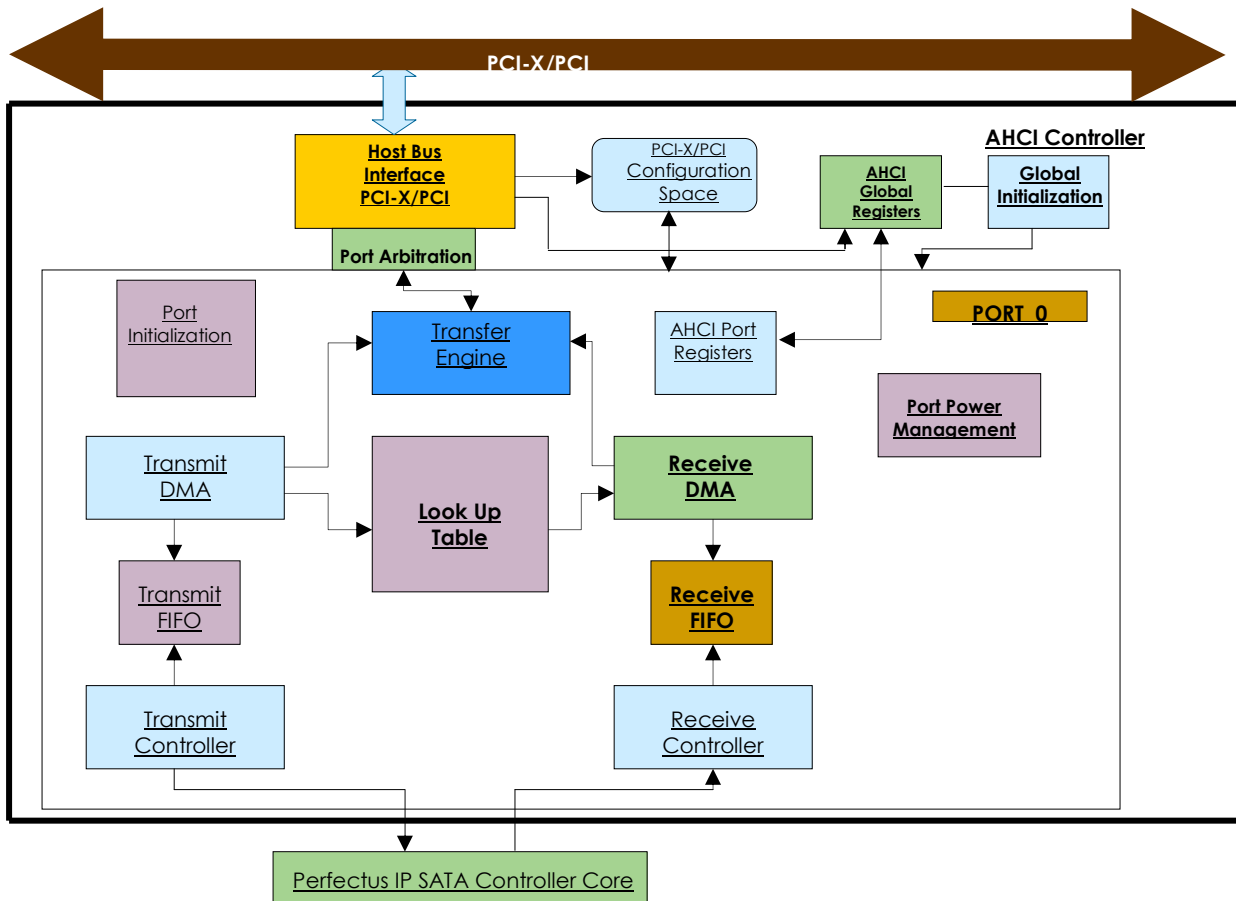
SATA-AHCI Design IP

SATA AHCI Controller Core

Overview

The Serial ATA (SATA) is a standard storage interface for serially attached storage devices. The Generation I (GEN-I) SATA is defined at speed of 1.5 Gbits/sec and the Generation II (GEN-II) is defined at 3.0 Gbits/sec. Perfectus introduces a SATA AHCI (Advance Host Controller Interface) Controller Core that can be easily integrated into SATA Host application. The SATA AHCI Controller from Perfectus adds a DMA layer on top of the SATA Core and creates a SATA Host solution. The core is register compatible with the AHCI 1.1 specification from Intel.

Figure 1: Block diagram





Features

- SAPIs Version 0.9 Compliant PHY Interface
- Supports NCQ
- Supports Port Multiplier and Port Selector
- Supports both PIO and DMA transactions
- Sits on top of Perfectus SATA Core
- Currently implements PCI-X as host interface at 133 MHz (But can be upgraded to any Host interface easily)
- Supports both Partial and Slumber Power Management modes
- Automated Self-checking test environment
- Operates Up to 133MHz Application Clock (Host clock)

Design Features

- Supports all the AHCI features
 - Support GEN1 (1.5 Gbps) and GEN2 (3.0 Gbps) speeds
 - Hot plug support
 - 64-bit addressing on PCI-X
 - Staggered Spin-up support
 - ATAPI Support
- Supports up to 32 outstanding commands per port
- Each command has its own DMA context
- Supports maximum of 16 ports
- Each port has its own set of registers and resources
- Generates interrupts to the CPU as per the settings
- Implements 64-bit PCI-X at 133 MHz

Deliverables

- Synthesizable RTL Code for the Core
- Test Environment
- Test Vectors
- Synthesis Scripts
- User Documentation
- Docs On Demand
 - LINT results
 - Code Coverage results
 - Test log files
 - Complete Test Suite
- Sample & Extensive tests covering basic functionality
- User Guide & release notes
- Fast bug fixing
- Online support service