



## Data Sheet

# Perfectus Verification IP SMBus

### Overview

The Perfectus VIP for SMBus provides an efficient algorithm to verify the SMBus based designs by giving the advance techniques including the support for System Verilog assertions.

The VIP comprised of BASIC TEST to verify the BFM. It also includes RANDOM TESTING to make the VIP more powerful. The monitor is used to track the bus traffic. It generates the LOG file to support the designers in verifying the VIP. The Checker is used for bug fixing inside the BFM. Various rules are implemented for checking the behavior model. The Perfectus VIP for SMBus includes the following:- SMBus master, SMBus slave, SMBus monitor and SMBus checker.

The Perfectus VIP also includes supports for System Verilog assertions which includes following:

- Functional assertions
- Timing assertions
- State Machine assertions

### Features

- Compliant to SMBus 2.0 specification
- Generates and drives bus traffic as a SMBus 2.0 Requester
- Responds to transactions as a SMBus 2.0 Slave comes as
- Generic and compatible with two wire serial EEPROM
- Commands and Knobs that change with every transaction
- Knobs to configure cycles
- Ability to carry over parameters across transactions
- For passing data
- For injecting different types of errors
- Ability to inject Packet Error Checking (PEC) error & protocol error
- Ability to inject error in any phase in a transaction
- Ability to add multiple errors in a cycle randomly

### Product Details

**SMBus Master:** SMBus master initiates transfer on the bus. User configurable knobs to support various features of master. The SMBus Master BFM supports the following Transfer types:

- Byte Read/Write with/without PEC
- Word Read/Write with/without PEC
- Block Read/Write with/without PEC
- Process Call
- Quick Command
- ARP

### SMBus Slave:

SMBus slave responds to the transaction initiated by the master. Storing ability as internal memory and supplying data on the demand.

- Configurable as general purpose Slave or Serial EEPROM
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- Supports ARP
- Configurable ACK/NACK on data phase

- Configurable to check PEC
- EEPROM loaded via File/user specified data

#### SMBus Monitor:

SMBus monitor generates LOG file and tracks the traffic of the bus. User configurable LOG file. Programmable file names for logging information. Also supports Performance Analysis and Functional Coverage.

#### SMBus Checker:

SMBus checker provides bus-level protocol checking capability. It performs real-time reporting of errors on the clock in which the End symbol of a packet is received

#### Benefits

- Supports back to back environment.
- Can be placed easily in any Soc Design.
- BFM commands are fully user configurable.
- Faster Test bench development and supports BASIC and RADOM Test cases.
- Executable in every major simulation environment.

**Test Bench Language:** Test case files are of two types in Environment.

- Text - Simple file controlling the knobs.
- Verilog - For more controlled test bench scenarios.

**Supported Platform:** Windows, Linux.

**Supported Simulators:** VCS 7.x, NCVerilog 5.x, Modelsim 6.x.

#### Deliverables

Perfectus deliverables includes:

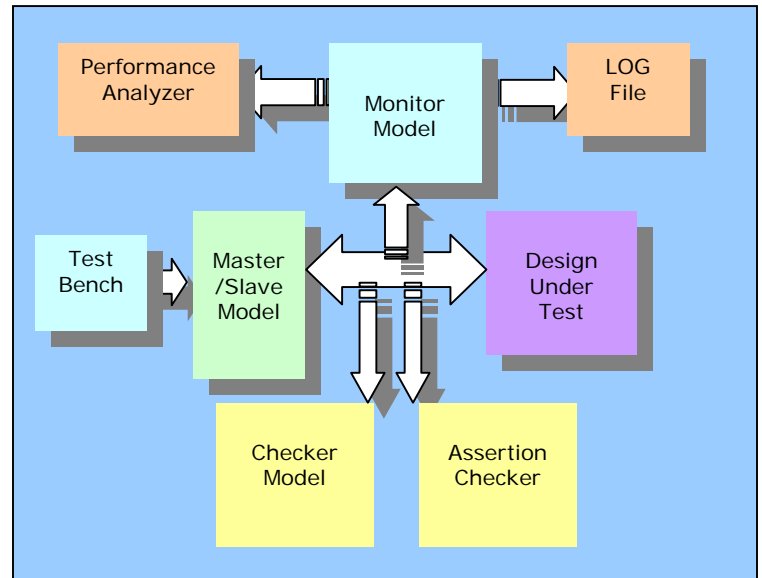
- Fully configurable BFM
- Sample & Extensive tests covering basic functionality
- User Guide, Assertion Document & release notes

#### Support & Training

- Fast bug fixing
- Online support service

- On demand training

#### Block Diagram



#### VIP for SMBUS System

#### About Perfectus VIP

Perfectus other Verification IP includes:

- SAS
- SATA
- AMBA: - AHB, APB & AXI
- OCP
- Fibre Channel
- AMB
- SM bus
- FBDIMM

Perfectus Verification IP support the various environments

- SystemC & SystemVerilog
- Verilog HDL & VHDL
- C/C++
- Vera & e

For more information visit our site

[www.perfectus.com](http://www.perfectus.com)