

DATA SHEET

USB 2.0

Genie-USB™ Verification IP

Overview

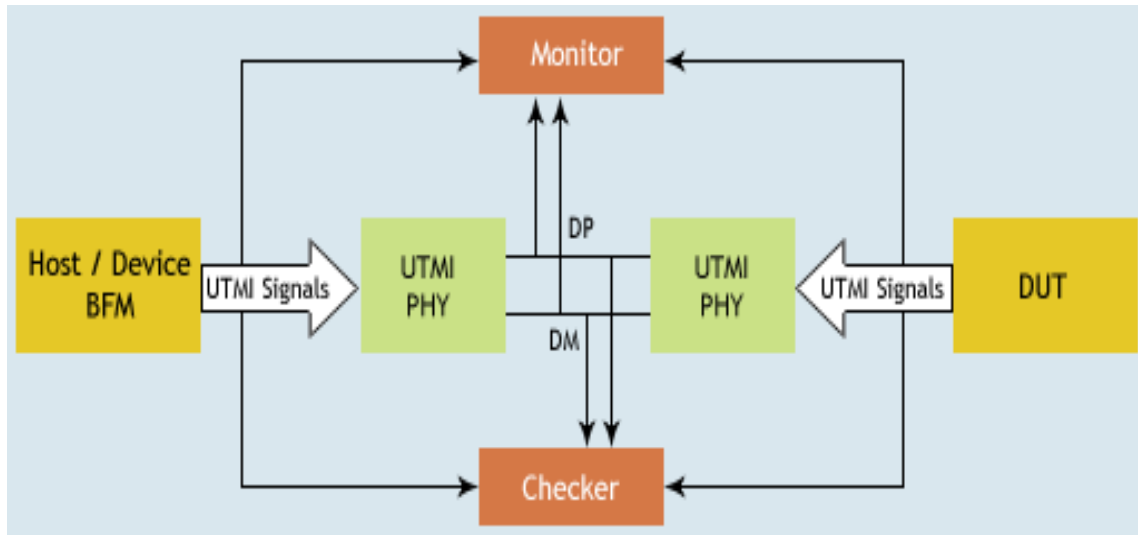
Genie-USB provides efficient comprehensive verification of USB2.0 based designs. The package includes USB Host, USB Device, Protocol Monitor (Independent entity) and a Protocol checker.

Genie-USB enables verification of designs at both transaction and packet levels.

Monitor is used to track the bus traffic on both HOST and DEVICE side. It generates LOG file to support the designers in verifying the Design. The protocol checker on-the-fly checks for protocol violations and reports errors. Various rules are implemented for checking the behavior model.

Genie-USB ships with Compliance Test suite extracted from every single line in specification. Verification-IP is written in native SystemVerilog language.

Figure 1: Block diagram



USB HOST:

USB HOST initiates all type of data transactions on USB bus. It has Programmable timers for suspend, resume, and reset signaling. User can introduce PID or CRC errors in the packet.

USB DEVICE :

USB Device responds to all commands issued by USB HOST either by accepting data or sending data. User can configure Device to send specific data. User can introduce errors in the packet.

USB Monitor:

USB monitor generates LOG file and tracks the traffic of the bus.

USB Checkers:

USB checker provides protocol-checking capability. During a transaction if any error occurs then it will log that protocol error.

TestBench Language:

Verification IP supports following testbench environment:

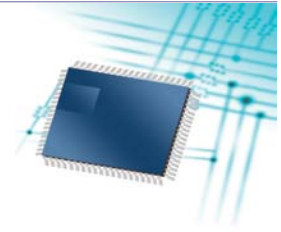
- System Verilog
 - Verilog
 - C/C++
 - VHDL
 - Vera
 - e
 - SystemC
-

Supported Platforms:

Windows, Linux and Solaris

Supported Simulators:

VCS 7.x,NCVerilog 8.x, Modelsim 6.x



About Perfectus

Perfectus other Verification IP includes :

- SAS 2.0
- SATA - II
- AMBA :- AXI,APB, AHB
- OCP
- USB 3.0
- PCI Express Gen2
- SPI 4.2
- Fibre Channel
- Ethernet 1G/10G
- SMBus 2.0

Perfectus Verification IP support the various environments:

- System C
- System Verilog
- Verilog HDL
- VHDL
- C/C++
- Vera
- e

Features

- Compliant to USB Specification Revision 2.0 (1.1 compatible) & supports OTG supplement to USB 2.0 Revision 1.0a
- Full timing, bus functional modeling of USB 2.0(Full/High/Low speed)
- Modes Host and Device
- Supports Link Power Management (LPM)
- Supports UTMI, D+/-, ULPI interfaces
- Supports OTG host/devices
- Supports Bulk, Control, Isochronous & Interrupt Transfer
- Protocol checking and transaction logging
- Direct access to configuration, reset, power, and state registers
- User - customizable packet generation
- Error injection capability

Benefits

- Supports back to back environment
- Can be placed easily in any Soc Design
- BFM commands are fully user configurable
- Robust & comprehensive verification of USB designs
- Faster Test bench development
- Executable in every major simulation environment